THEORY of OPERATION
GPx200

GENERAL -- The GPx200's are quad-output 200W power supplies. The key features of this series of off-line switching power supplies are as follows;

1) Wide-range AC input voltage - 85 to 264 Vac,
2) MOSFET based, current mode PWM converter stage,
3) Fixed operating frequency - ~ 62 kHz,
4) Compliance with FCC and VDE Class B conducted EMI,
5) Most outputs independently regulated,
6) All outputs short-circuit protected,
7) Output #1 is adjustable with overvoltage protection,
8) Rated to operate from 0 to 50 deg C. with forced convection required above 150 W continuous.

Note: This description of circuit operation assumes a very basic understanding of power rectifier circuits and current mode pulse-width modulation (PWM) operation. Additional information can be provided, subject to the constraints of proprietary information disclosure.

AC INPUT / RECTIFICATION

The input voltage is applied to the EMI filter through the fuse (F1). The input voltage must be AC, 85 to 264 Vac, of 47 to 63 Hz, with less than 5% distortion. The input fuse provides protection from fire hazard under catastrophic failure conditions. Under normal conditions, the control circuits provide overcurrent protection. Moderate energy voltage transients on the input power are clamped by a metal oxide varistor (M1). The MOV clamps excessive non-repetitive voltage transients of less than 250 microseconds duration and limited to 10 Joules of total energy. Input current then passes through a common-mode EMI choke(s) (T1,2,5) with both common mode (C3,4) and differential filter capacitors (C1,2) from line-to-ground and line-to-line respectively. These components attenuate switching frequency and rectifier harmonics to within the FCC and VDE class B limits for conducted emissions. Peak inrush current is limited by series negative temperature coefficient (NTC) thermistors to approximately 65 Amps peak @ 240 Vac. Current flow though RT1 & 3 raises the temperature of the thermistors, reducing their resistance and the inherent voltage drop across the thermistor to less than 1V. The bleeder resistor (R1) across the AC mains is provided to discharge the EMI capacitors when the AC power is interrupted. The input voltage is then rectified through a full-wave bridge rectifier (CR1) and filtered by large electrolytic capacitors (C5,6) to provide DC voltage with a small ripple voltage at twice the input frequency. The peak ripple component is typically 0 to 20% of the peak input voltage.

SWITCHING CONVERTER STAGE OPERATION

The switching converter stage chops and transforms the high voltage DC bus at C5,6 to multiple low voltage outputs. The DC bus voltage is always applied to one end of the primary winding of the power transformer (T3). The drain of the power MOSFET transistors are connected to the other end of the primary winding. When the control circuit provides gate voltage to the power switches (Q1,2,3), the entire input voltage is applied across the primary winding. Current begins to ramp up from the initial level set by the flux remaining in the core at a rate proportional to the input voltage. Power is not transferred to the output windings during this portion of the switching cycle since the primary winding is out of phase with the secondary windings. Reverse current flow is blocked by the output rectifiers. Thus, the power to be transferred to the outputs must be stored by the power transformer.

Energy storage is possible since the power transformer is actually an inductor with multiple windings. Once the stored energy reaches a level determined by the control circuit, the gate voltage is rapidly removed from the power switch gates, switching them off. The interruption of current flow in the power transformer forces the voltage across the primary to reverse almost instantaneously, rising to the level required to provide a discharge of the flux built up in the power transformer. Since the secondary windings are out of phase with the primary, the voltage across the windings must reverse and rise to the lowest clamping voltage of any winding. The action of the transformer is said to "fly back" to the clamping level, thus the popular term flyback converter. The clamping of the transformer primary is not perfect. The short time after the current in the primary is interrupted and before the secondary current has overcome the leakage inductance of the output windings leaves the primary unclamped to any voltage. The end of the winding attached to the power switches will rise rapidly, trying to discharge the energy stored in the power transformer. Left unclamped, the rising voltage could avalanche the power switches leading to their failure. A temporary path for current in the primary winding back to the DC bus exists through the primary snubber, (CR2 and C7). The snubber slows the rising voltage, allowing the output current to reach its peak value. Bleeder resistors (R3,78) discharge or reset C7. The result is a sawtooth waveform across C7 of approximately 100V pk.

The primary current is sensed by the 100:1 current transformer (T3), with the voltage signal restored by current flow through CR32 and R28. The control circuit monitors the voltage analog of the primary current and shuts off the power switches early if excess current is detected (approx. 1V peak).

OUTPUT RECTIFIERS, FILTERS and POST-REGULATORS

Output #1 -- The output rectifiers (CR11,22) clamp the transformer windings directly to the filter capacitors (C28-32,42,43,57) for the +5V output. The output capacitors receive charge from the power transformer during the power transistor "Off" time or flyback period. When the power transistors turn "On" again, the output capacitors must provide all the output current. The reversal of current flow into and out of the filter capacitors causes a small voltage ripple on the capacitors. A secondary ripple filter (L3 and C35,72) is used to reduce switching spikes and ripple to acceptable levels. Small capacitance and inductance can cause reverse voltage spikes in excess of the rating of the rectifiers. To snub the spike voltages to acceptable levels, a dissipative snubber (R26 and C45) is connected across the anode to cathode of CR11 and CR22.

Output #2 -- Output #2 is regulated by a saturating choke or magamp (L1) in series with the transformer and output rectifier / filter. The transformer winding is capable of providing approximately 25% excess voltage to the output. The magamp blocks current flow to the output for a portion of the flyback cycle based upon the level of reset received during the preceding forward portion of the switching cycle. Since the output appears to be an open circuit, the transformer clamps to one of the other outputs at a higher voltage per turn. Once the magamp saturates, practically all the current flows into the filter capacitors of output #2 (C34,39) through the rectifier (CR5). L2 and C40,44 provide a ripple and noise filter. R23 provides a preload. Before the next cycle, the magamp must be reset to the appropriate level. Magamp reset is discussed in the Control Circuit section. (Reference: Magamp Output Regulator Reset Control).

Output #3 -- Output #3 is a conventional output filter with a spike blocking choke with active reset (R35, CR26 and L8) added to prevent overcharging of C38 under certain conditions. CR17 rectifies the negative output voltage at C38 during the flyback cycle. L6 and C33 provide additional ripple attenuation for the input voltage of U4. U4 can be either a fixed or programmable 3-pin linear regulator. The input voltage must be more negative than the desired output voltage level (typically 2.7 to 6 Vdc). The regulator then blocks the additional voltage to provide good dynamic and load regulation (< 1%). If a programmable regulator is used, R29 and R60 provide an output voltage divider with 1.25Vdc across R60 and the balance of the desired output voltage across R29. R33 provides preload while C26 and C41 provide noise filtration. CR7 and CR16 are for reverse voltage protection.

Output #4 -- Output #4 is another magamp controlled output similar to output #2. The magamp choke, L5, blocks excess voltage for part of the flyback cycle, then saturates and provides charge through CR19 to C20. Ripple and noise filtering are provided by L7, C21 and C22. Preload is provided by R68. The control circuit is almost identical to that of Output #2. (Reference: Magamp Output Regulator Reset Control)

CONTROL CIRCUITS

Main Output Regulation and PWM Operation -- The main output voltage (#1) is controlled directly and thus sets the transformer voltage for all the other outputs. The output voltage is sensed through the resistor divider R36, R53 and R54. The potentiometer, R53 adjusts the voltage ratio applied to the reference of U6 (2.50V reference). When U6-R is above 2.5V, the cathode pin conducts current through the optocoupler photodiode (U2). The current in the photodiode of U2 causes base current to flow in the output transistor of U2 which pulls down pin 1 of U1. At approximately 1V on U1-1, the output pulses are at minimum width. If the pulse width is too narrow (Output #1 too low) less collector current flows through the photo transistor of U2 allowing U1-1 to be pulled up to the 5.00V reference of U1 (Pin 8) by R9 increasing the pulse width to a maximum of approximately 47% "On" time.

Modulation of the pulse width occurs inside U1. A flip-flop is set as the timing cap (C11) begins to charge through R10. If the voltage at U1-1 is of sufficient magnitude, the output driver goes high at the same instant (U1-6), turning the power transistors "On". The primary current begins to ramp. The current signal is compared to a portion of the voltage at U1-1. When the ramp reaches the level of U1-1, the output driver is latched "Off". The timing capacitor continues to charge to approximately 3.3V. Once this level is reached, U1-4 switches to a rapid discharge mode back to 1.6V. The timing oscillator repeats the same cycle with the output driver latched "Off" by an internal flip-flop that is reset by the oscillator cap discharge. Thus, the oscillator operates at twice the actual power switching frequency and the maximum duty cycle cannot exceed 50% (typically less due to the discharge time of the timing cap).

Primary and Output 1 & 2 Overcurrent Protection -- Excessive current, (voltage at U1-3 more than 1V) causes the output driver to switch off and latch until the next normal "On" pulse. The current limit inherent to the chip will hold the primary current to a given peak current, but the power dissipation could be excessive if left in this condition indefinitely. An external shutdown circuit prevents damage during sustained short circuits or overloads. When the current limit pin assumes control of the PWM, Pin 1 begins to rise to 6V (supplied by an internal current source). The phototransistor of U2 ceases shunting current since the output voltage is to low due to the output overload.

Once the voltage at U1-1 goes above 5V, the voltage at U7-Ref rises to 2.5V causing the cathode to begin conducting current, turning Q12 "On". Current flowing from Q12-Collector provides positive feedback to U7 and pulls U1-3 above 1V, latching the output driver (U1-6) "Off" stopping all power switching. The Bias voltage (TP1 to TP5), decreases to the undervoltage lockout point of U1 (approx. 10V), turning U1 "Off". The startup capacitor begins to recharge through R2 until the start-up threshold is reached (approx. 16V). Normal switching operation will commence if the fault has been removed. If the fault is still present, the shutdown cycle will repeat. The power supply thus appears to be providing short bursts of power or "hiccuping".

Magamp Output Regulator Reset Control -- (The description that follows refers to Output #2.) The magamp inductor blocks practically all current flow in the output until the it saturates. By varying the reset point of each pulse (volt*second product required to saturate the choke), tight voltage regulation is possible. The reset is accomplished by controlling the reverse, or reset current through the choke during the power switch "On" time (output winding reverse biased). Current is provided by the current source formed by a PNP transistor and power resistor (Q13 and R4, respectively; reference Output #2). The output voltage is sensed by the resistor divider of R20, R21 and R22. The control voltage at the reference of U3 is maintained at 2.50 Vdc by shunting additional current into the anode when the voltage is too high. Increased current through R5 and R15 increases pulls the base of Q13 further below the output voltage rail, thus increasing the reset current provided to the magamp choke. CR6 provides reverse bias protection for the control circuit when the magamp is conducting current to the output filter capacitors. CR21 helps to stabilize the current source by providing a continuous path for current during the forward bias cycle of the power transformer.

Overvoltage Protection -- If the voltage of the main output increases beyond safe limits, the overvoltage protection zener diode begins to conduct (CR12). When sufficient current is available to raise the gate of SCR1 to approx. 0.7V, the SCR latches "On", shorting the output causing a "hiccup" cycle that will repeat until the fault is removed or the power supply is repaired.

Overtemperature Protection -- The chassis temperature is sensed by a PTC thermistor mounted along the side. When the chassis rises above approx. 90 deg C, the resistance of the PTC increases rapidly, raising the base of Q7 to the point of conduction. Q7's collector shunts current from the output through the voltage control optocoupler (U2) lowering the output voltage and power. If the chassis temperature does not stabilize or begin to drop, the output will continue to pull down until the Bias voltage for the primary control circuit is lost initiating "hiccup" mode.

Power Fail -- The power fail signal monitors the voltage of the input storage capacitors (C5 & 6) as reflected by a transformer winding. When the transformer is switched "On" across the bus voltage, the main output winding is reverse biased. The peak voltage of the main output winding is captured by C37 through CR15. Thus a negative secondary voltage proportional to the input bus voltage is generated. This voltage is summed with the main output voltage at the base of Q8 (input of the differential amplifier). As the input bus voltage rises to a less negative level, Q8's base becomes forward biased from the main output voltage. As Q8 conducts, Q10 turns "On", dropping the Power Fail signal to less than 0.5V. The signal thus becomes active Low any time the bias to Q8's base is present. Therefore, raising the factory setpoint of the main output voltage may require resetting the Power Fail trip-point. The signal typically falls at least 5 mSec prior to the bus voltage dropping below the point where the full output voltage can be sustained.

Note: This signal operates based upon the actual voltage present at the input capacitors. AC waveforms with substantial distortion (e.g., Variac impedance clipping) may cause the Power Fail to activate at a higher RMS value of input voltage. The GPx200 power supply specifications assume usage with sinusoidal AC input voltage. If the Power Fail is set to activate at lower input voltages, less warning time will be available prior to loss of main output regulation.